Exhibit

PB 02 0018

INVENTION QUESTIONNAIRE

Date: 04/03/02

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Specific product where your invention will or most likely be implemented (e.g. TITAN 6500).
(NPI) ALL TEST ENGINEERING FUNCTIONAL TEST INTERFACES TITAN 5500 6500

Feature package and release date, if applicable, (e.g. FP1.0 – to be released 1/31/02; no feature package determined yet, etc.):

Other products or applications where your invention may be implemented:
ALL PRODUCTION SWITCH & PORT COMPLEX SHELVES/BACKPLANES

Your Sales/Geographic region (e.g., North America): NORTH AMERICAN

What is the title of your invention?
ELECTRONIC INSERTION/EXTRACTION CYCLE COUNTER AND LOGGER DEVICE.

What is your invention in "simple terms"? (e.g. what is being patented -- a method/process/algorithm for synchronizing network elements, an apparatus for synchronizing network elements)
AN ELECTRONIC DEVICE USED FOR KEEPING COUNT OF THE NUMBER OF INSERTION/EXTRACTION CYCLES OF BACKPLANE CONNECTORIZATION IN SWITCH AND PORT SHELVES

To what technology does your invention generally relate?
BACKPLANE CONNECTORIZATION OF SWITCH & PORT TELCOM SHELVES BOTH ELECTRICAL AND OPTICAL

Describe the problem your invention is trying to solve:
HIGH DENSITY BACKPLANE CONNECTORS MATING CYCLES CAUSE WEAR IN THE FORM OF MECHANICAL & PLATING OF THE CONNECTOR CONTACTS. THIS WEAR CAN CAUSE INTERMITTANT FAILURES CAUSED BY POOR ELECTRICAL CONNECTIVITY AT THE CONNECTOR. THIS DEVICE KEEPS TRACK OF THE INSERTION/EXTRACTION CYCLES TO WARN THE SYSTEM OF A POSSIBLE WORN CONNECTOR. ALSO, THE REQUIRED CLEANING/MAINTAINANCE CYCLES FOR OPTICAL CONNECTORS MAY BE MONITORED

Describe prior approaches in the industry to solve this problem and the inadequacies of these approaches:
TO THE BEST OF MY KNOWLEDGE NO ONE HAS ADDRESSED THIS PROBLEM, other than preventive MAINTANENCE CYCLES PERFORMED ON CONNECTORS ON A "AS NEEDED" BASIS.

BEST AVAILABLE COPY

Describe advantage(s) of your invention over prior approaches in the industry:
PRIOR APPROACHES IN THE CONNECTORIZATION INDUSTRY HAVE BEEN TO IGNORE THIS ISSUE DUE TO THE ASSUMPTION OF MINIMAL INSERT/EXTRACT CYCLES THROUGHOUT THE BACKPLANE LIFE CYCLE. THIS APPROACH WOULD BE NEW IN THE CASE OF BOTH ELECTRICAL AND OPTICAL CONNECTORIZATION MONITORING.

Describe in detail how your invention works:
THE CONNECTOR USAGE COUNTER IS CONTAINED ON A SMALL PCB (PRINTED CIRCUIT BOARD) OR INCORPORATED ON THE BACKPLANE ASSEMBLY A SMALL EMBEDDED MICRO-CONTROLLER THAT CONTAINS NON-VOLITAL FLASH MEMORY KEEPS TRACK OF THE NUMBER OF TIMES A MODULE IS INSERTED/EXTRACTED FROM THE BACKPLANE ASSEMBLY. THE COUNT IS INCREMENTED BY ONE EACH TIME AN ELECTRICAL CONNECTION IS MADE THROUGH A SPARE PIN ON THE MONITORED CONNECTOR OR FOR OPTICAL THROUGH A SENSOR LOCATED NEAR E

Who is likely to want to use your invention or infringe a patent on your invention?
ANY TELCOM OR LARGE SYSTEMS COMPANY THAT USES MANY ELECTRICAL AND OPTICAL CONNECTORS IN THERE FIELD PRODUCTS.

How easily could Tellabs independently detect another's use of your invention?
PATENT SEARCH FROM CONNECTOR COMPANIES, TELCOM COMPANIES

Illustrate your invention in one or more figures (e.g., if your invention pertains to software, provide a flowchart). Please attach all illustrations with this invention submission and e-mail to: Janet.Missig@tellabs.com

List by name all persons who may have contributed to your invention. (If any such person is not a Tellabs employee, indicate their relationship to Tellabs.)
JEFF HOTZ (MANAGER) MARY LOMAS - SALES REP TERADYNE CORP.

per M.Inlow, M.Lomas did not contribute to the invention, she only has knowledge of it.

To help prevent loss of patent filing rights, a written non-disclosure agreement (NDA) should be obtained prior to any disclosure or demonstration of your invention to individuals or entities outside of Tellabs (e.g. trade show, field trial, demo for a customer, fabrication instructions to a vendor). An NDA may be requested through the Tellabs internal legal web site:
`http://legal.hq.tellabs.com/contracts/templates/nda/index.asp`

Has your invention already been or will be in the future:

- disclosed or demonstrated
- published or submitted for publication
- sold or offered for sale

to individuals or entities outside of Tellabs?

If so, describe the circumstances, addressing: date(s), individuals or entities involved, countries involved, reasons, existence/non-existence of NDAs.
MARY LOMAS FUNCTIONAL TEST SOCKET SAVER'S FOR TEST BACKPLANES SHE HAS NDA WITH TELLABS & TERADYNE

Does your invention relate directly to technology that is/will be/might be the subject of an industry standard, or does your invention otherwise relate to technology that is/will be/might be of interest to a special interest group of any sort?
NO

Your supervisor's name: PHIL GASNER

Indicate whether your supervisor is aware that you are submitting your invention for review by the Tellabs patent committee: Yes: X No: __

Your comments on this invention disclosure form and the Tellabs patent process are greatly appreciated:

Review pending: ______ Reviewed by: ______

Reviewer's notes:

Signature

Dated 07/08/02

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Work Instruction

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Connector Counter Hardware Description Document	05.5014.4149	AP2	10/24/01
Subject	File Code	Rev	Effective Date

Functional Hardware Description Document

and Firmware Programming Instructions

for

Connector Counter 80.6511

Approvals					
Title	Signature	Date	Title	Signature	Date
Author Mark Inlow					
Manager Jeff Hotz					

Work Instruction

REVISION HISTORY

Issue	Date	Change Description	Originator
A	02/15/01	Original Release.	Mark C. Inlow

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4. Calibration and Preventive Maintenance

There is no calibration required for the Connector Counter PCB. Preventive maintenance is not required for the Connector Counter PCB.

5. High-Level Connector Counter Hardware Description

The CC uses a PIC micro controller port to interface with the UUT via a 28 pin header located on the rear of each test interface. Pin 5 brings the count signal from the UUT. Future designs also may incorporate this counter design on the test interface itself, eliminating the need for a separate daughter card. The CC is composed of a custom Test Engineering PCB that connects to the test interface backplane via a 28 pin header. The functional test interface provides the necessary power and signals to communicate and control the CC. The following is a listing and description of the CC's hardware blocks and electrical interconnects. Refer to Figure 1 for a block diagram of the interface. The sections below describe each block.

5.1 Count Input Conditioning

The UUT provides a ground (low) when the UUT is inserted into the test interface. The test interface designer should use either the MODULE PRESENT signal available on most new product module designs. If this signal is not available, simply pick one digital ground pin on the UUT connector, isolate this from ground on the test interface, and route this signal to the CC's 28 pin header pin 5. This signal is routed through the 28 pin header from the test interface backplane to a 49.9 ohm series current limit resistor. This line is pulled high with a 10K ohm pull-up resistor. CR1 clamps unwanted transients. C2 filters out spikes which could cause false counts. The count input signal is routed to the uC port RB4 configured as an input.

5.2 Address Switches

There is a four position DIP switch with one side of each switch tied to +5 VDC and the other side of each switch has an associated pull-down resistor which is also connected to the uC ports RA0 through RA3. The switches set the HEX address of the CC which is read by the uC at power on reset. Any unique address may be chosen in the range of 00H to 0xFFH. There is no default.

5.3 Power Fail Detect Circuit

The +5 VDC supply voltage derived from the test interface backplane is monitored by a Dallas Semiconductor DS1811R-10 5V EconoReset IC with an open drain output which is pulled high via a 10K ohm pull-up resistor. The DS1811R's output which is connected to port RB0_INT of the uC is set to transition low when +5 VDC falls below 4.35V (typical). This high to low transition causes a hardware interrupt to the uC which its firmware then saves the current insertion count from RAM to non-volatile EEPROM.

5.4 Microprocessor and Clock Oscillator

The microprocessor implemented in the CC design is a Microcip Technology Flash based micro controller with 1024 words of program memory, 68 bytes of data RAM, 64 bytes of EEPROM and 13 I/O port pins capable of sinking or sourcing 25 MA of current each. There is also an internal power-up reset circuit, two general purpose programmable timers and four interrupt sources. The uC can operate down to a supply voltage of 2.0 VDC. The uC clock is derived from a parallel cut 11.059 MHZ crystal connected to the uC's OSC1 input and OSC2 output respectfully. Two external capacitors are connected on each side of the crystal to provide increased stability of the oscillator. The values were chosen based on the manufacturers recommendations. The 11.059 MHZ clock is internally divided by four to provide a 36.2 nanosecond instruction cycle.

5.5 RS232 / RS485 I/O Port Drivers

Serial communications to and from the CC are provided by the uC ports and level converted to the RS232 standard utilizing a Maxim Semiconductor MAX232A IC. The IC provides the +/-9 VDC required from an internal charge pump circuit and four external electrolytic filter capacitors. The TX and RX signals are routed to the 28 pin header to allow connectivity to the test interface backplane directly or are available at an on board RJ11 jack. If multiple CC's are required to keep track of the connector count on multiple test interfaces, a Linear Technology RS485 transceiver LTC485 is also connected to the uC serial port lines and is available at both the 28 pin header and the RJ11 jack. Depending on the address switches set on each CC, response occurs only on the RS485 bus when the CC sees its unique address.

5.6 LED Status Indicators and ISP Port

There are three LED status indicators provided on the CC. These are sourced from three uC ports. These lines are also routed to the 28 pin header if the test interface should require to read the status directly.

1) The "AWAKE" LED illuminates green when the uC comes out of "sleep" mode.

2) The "ADDR DETECT" LED illuminates red when the CC is communicated with and its own address matches.

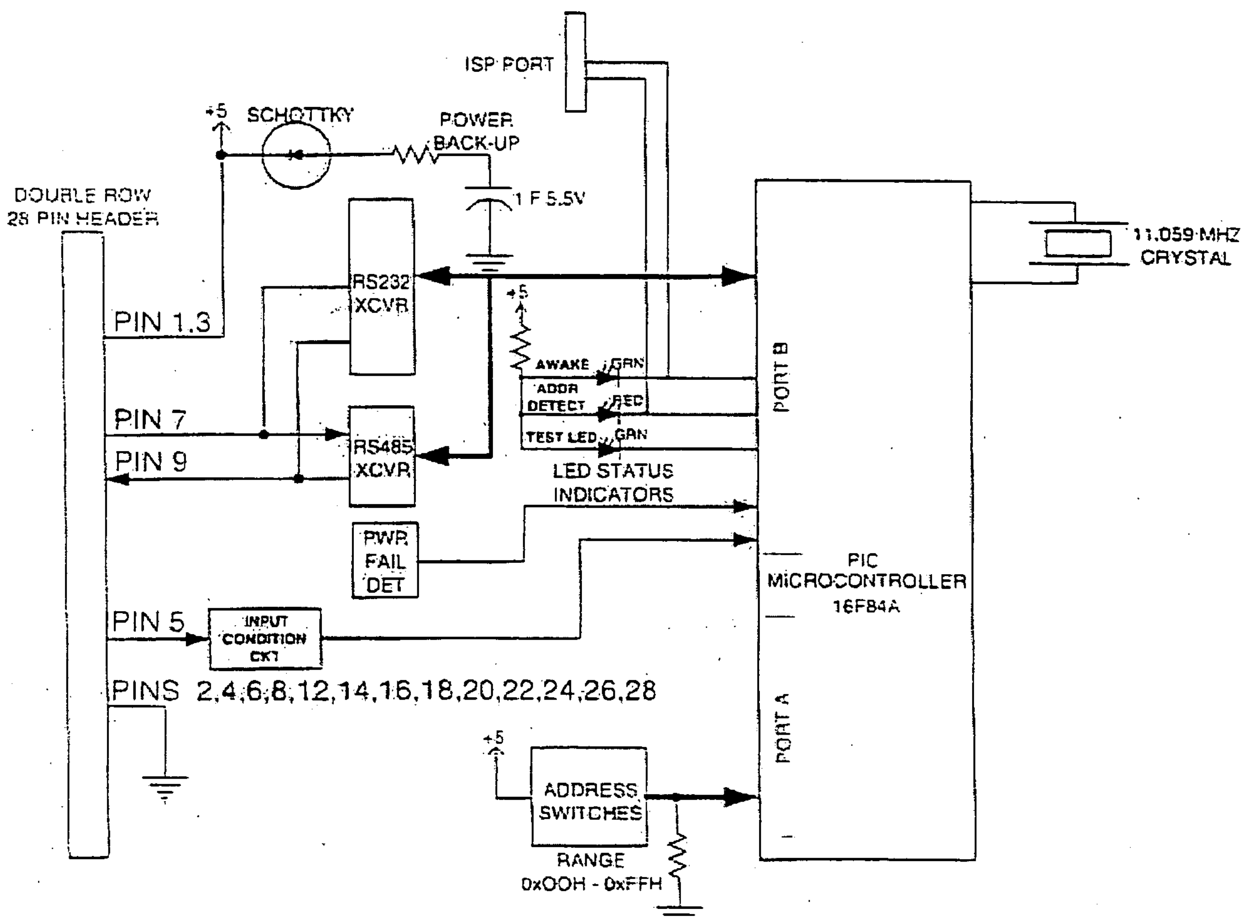
3) The "TEST LED" is a spare LED available for debug and future designs.

The firmware program for the CC contained in FLASH within the uC may be programmed through the ISP port connector P2. This connector provides the necessary programming signals to the uC pins from a Microchip PIC device programmer or OEM equivalent.

5.7 1 Farad Backup Capacitor

The test interface is powered down and +5 VDC is not available until just before the functional test starts. If the operator plugs the UUT into the interface before power is applied an insertion count would be missed. To correct for this problem a large value low leakage capacitor is used to keep power available to the CC from the last test. A 1 Farad 5.5vdc rated capacitor and 82 ohm series charge resistor provide 5 VDC to the uC. This capacitor charges to approximately VCC (+5 VDC) through the 82 ohm current limit resistor. This limits the inrush current of the capacitor as power is applied. This voltage supplies the uC only through a steering schottky diode. This limits the current draw on the capacitor to the uC only for optimum charge time between tests.

Figure 1. 80:6511 Connector Counter Block Diagram



6. Reference Section

6.0.1. uC Port I/O Bit Definition

Table 8: uC Pin Definition

I/O	Function
RA0	CC address select input ADDR0
RA1	CC address select input ADDR1
RA2	CC address select input ADDR2
RA3	CC address select input ADDR3
RA4_TOCKI	Unused input (pulled high)
RB0_INT	Power Fail Detect interrupt input
RB1	"AWAKE" LED indicator output
RB2	Serial TXD output
RB3	Serial RXD input
RB4	Connector insert/extract input
RB5	RXD Start Bit interrupt Detect input
RB6	"TEST" LED indicator output
RB7	"ADDR DETECT" LED output
MCLR	Power-on clear input (pulled high)

6.1 Firmware Description

The firmware of approximately 400 words long is stored in the 1024 word flash memory within the uC. The firmware is programmed into the uC via an ISP programming cable and a Microchip Picstart Plus development programmer or equivalent. Briefly, the firmware program performs the following functions. At power-up reset all the I/O ports are initialized as well as the uC internal registers. The interrupts are enabled and the address switches are read. The insertion count value that was in the EEPROM is also read and is used to update the RAM count location. The program then goes into a "sleep" mode which powers down the uC clock oscillator but leaves the current I/O port values as they are. This limits the uC current draw down to a few microamps and also keeps any unwanted uC 11.059 MHZ clock noise from affecting the UUT during the functional test.

The uC "awakes" from sleep mode upon receipt of a start character (high to low transition on port RB5). The program then loops until a full serial character is received. The CC looks for and acts on the following serial commands from the funtional test CVI calling program. Each command shall be proceeded by the HEX address of the CC being talked to and terminated by a carriage return character (HEX 0x0d).

xx = hex address of CC being address in the range of 00 to ff HEX.

CR = carriage return character (HEX 0x0D)

1) xxclear(CR) - Clears the CC's current insertion/extraction count to zero.

2) xxread(CR) - Reads the CC's current insertion/extraction count.

The program also responds to interrupts from the following sources and the uC "awakes" from each.

1) An insertion/extraction detected. The insertion/extraction count is incriminated by 1.

2) When +5 VDC falls below 4.35 (typical). The current insertion/extraction count is saved in EEPROM.

3) Time-out of the uC timer (tmr0) used to produce debounce delay of the insertion/extraction input.

The uC also enables a watchdog timer with a time-out value of 2.3 seconds. The main loop of the program clears the watchdog timer count value before it times out during normal program operation. If a serial communication failure or other program corruption from a power glitch occurs the watchdog times out and causes a hardware reset. This keeps the CC from ever "hanging up" and not responding.

7. Configuration Management of Microchip Files

Microchip files are under configuration management and are located on **tlabbd-8** in the digdoc/docs/microchip directory. General Microchip Files (*used by Test Engineering for Development*) are stored here as zipped files. The filename of the zipped file is the revision level. Hardware documents will refer to this revision filename as the current configuration data required for the Microchip device.

To retrieve a specific revision level of Microchip configuration files, use either a NFS connection or FTP client to map to tlabbd-8 digdoc/docs/microchip directory. Select the desired Microchip zip file (i.e. con_ctr1.ZIP) and copy to the workstation where Microchip Mplab software is running.

There are two options to UNZIP the Microchip files:

Option 1:

Copy the zipped file to your UNIX directory and use the UNZIP command. This will create the Microchip file directory in your UNIX account containing the unzipped files.

Path to ZIP/UNZIP Utilities is /usr/local/gnu/bin

Example: sunk44> unzip con_ctr1.zip

This will explode the Microchip files in a directory called con_ctr1/. Then use NFS or FTP client to copy over to the PC workstation. It would be wise to create a separate directory containing these files. Remember the location of the files when using the Mplab software.

To view the contents of a zipped file in UNIX type the following:

sunk44> unzip -l con_ctr1.zip (*The -l will list the contents of the file*)

Option 2:

Copy the zipped file directly to the PC workstation using NFS or FTP client and use the PKUNZIP utility. Be sure that the PKUNZIP.exe is available on the workstation.

After the zipped file has been copied to the workstation, open a MS-DOS prompt window. Now change to the appropriate directory where the zipped file exists.

cd\users\john_doe (*directory where con_ctr1.zip exists*)

Example: c:\users\john_doe> pkunzip con_ctr1.zip

This will explode the Microchip files in a directory called c:\users\john_doe\con_ctr1. Remember the location of the files when using the Microchip Mplab software.

For additional information on Test Software Release and Revision Control see 05.0012.0000

7.1 Firmware Programming Instructions

The following set of instructions are provided to assist Test Engineering or Lab Services in programming the required firmware into the CC.

The following items are required for programming:

1) Microchip Corporation Picstart Plus REV. V1.50 or greater and PC based software
2) PC running windows NT or Windows 98/2000 with Microchip Mplab software development tool installed. (This is available from Microchip Web site at no cost).
3) Tellabs built ISP adapter cable (Figure 2)
4) Insertion counter module 80.6511 to be programmed

To Download Firmware:

1) Install Mplab if necessary on PC. Invoke Mplab.
2) Go to *PICSTART Plus* pull down menu. Choose *Enable Programmer*
   Three windows appear,
   PICKSTART Plus Programmer Window
   Program Memory Window
   Configuration Bits Window
3) Under ***Debug*** pull-down menu, choose ***Clear Program Memory***.
4) Click yes to "***Do you want to fill all program memory with 0x3FFF?***"
5) Under the ***File*** pull-down menu, choose ***Import-Import to Memory***
6) Find the hex file named **con_cntr.hex** located in the directory created containing the un-zipped files described in the above *Configuration Management* section. Click OK
7) After the file is loaded the Program Memory Window will change to show the HEX program code.
8) Insure that the current checksum specified in the assembly drawing is displayed, and that the device type selected is **PIC16F84A**
9) Connect the CC to the PICSTART with the adapter cable, observing proper pin polarity at both the ISP port side and the PICSTART side.
10) At the PICSTART Plus Programming Window choose the Program button. Wait for the part to finish being programmed. Note the checksum and insure that it agrees with the current checksum.
11) Blank PIC16F84A IC's (PN TE270041) may also be pre-programmed prior to being placed on the PCB assembly by eliminating the adapter cable and placing the blank part directly into the PIC programmer
12) This completes the CC Flash programming. Remove adapter cable from CC.

Figure 2. ISP Adapter Cable Definition